

ABSTRACT OF THE DISCLOSURE

A method of operation of a memory controller device, the method of operation comprises issuing a write request to a memory device 5 synchronously with respect to an external clock signal, wherein in response to the write request, a memory device inputs first and second portions of data. The method of operation further includes outputting the first portion of data synchronously with respect to a first edge transition of an external clock signal; and outputting the second 10 portion of data from the bus synchronously with respect to a second edge transition of the external clock signal. The first and second edge transitions of the external clock signal are of transitions of the same clock cycle.